REMARKS

This application is a divisional of U.S. patent application number 09/808,114, filed March 15, 2001, and entitled TECHNIQUE TO MITIGATE SHORT CHANNEL EFFECTS WITH VERTICAL GATE TRANSISTOR WITH DIFFERENT GATE MATERIALS, the entirety of which is incorporated by reference in the present application. Claims 1-67 are cancelled as allowed in the parent application. Claims 68-91 are now pending.

Each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: January 28, 2004

Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Ryan H. Flax
Registration No.: 48,141
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorney for Applicants